WHAT IS CLAIMED IS:

1. A semiconductor device having an SOI structure including a semiconductor substrate , a buried insulating layer and an SOI layer , comprising:

a MOS transistor provided in an element formation region of said SOI layer; and

a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region to be a part of said SOI layer present in a lower layer portion of said SOI layer,

said MOS transistor including:

source and drain regions of a first conductivity type selectively formed in said SOI layer , respectively;

a gate electrode having a gate electrode main part formed through a gate oxide film on a region of said SOI layer between said source and drain regions; and

a body region having a body region main part to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion electrically connected from said body region main part in said element formation region and capable of externally fixing an electric potential.

2. The semiconductor device according to claim 1, wherein

said body region potential setting section includes a body region source/drain adjacent portion in a gate width direction adjacently to said source and drain regions and

extended in a gate length direction from said body region main part; and

said gate electrode further has a gate extension region extended in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, and serving to electrically block said body region source/drain adjacent portion and said source and drain regions through said gate extension region.

3. The semiconductor device according to claim 2, wherein

said body region source/drain adjacent portion includes a first body region source/drain adjacent portion extended in a first direction from said body region main part and a second body region source/drain adjacent portion extended in a second direction opposite to said first direction from said body region main part, and

said gate extension region includes a first gate extension region formed on a vicinity of said first body region source/drain adjacent portion and a second gate extension region extended on a vicinity of said second body region source/drain adjacent portion.

4. The semiconductor device according to claim 2, wherein

said body region source/drain adjacent portion includes one body region source/drain adjacent portion, and

said gate extension region includes one gate extension region formed on a vicinity of said body region source/drain adjacent portion.

5. The semiconductor device according to claim 2, wherein

said body region source/drain adjacent portion has a high concentration region

having a higher impurity concentration of a second conductivity type than that in other regions over a region provided apart from said gate extension region by a predetermined distance.

6. The semiconductor device according to claim 2, wherein

said gate extension region includes a gate extension region having an impurity concentration of the second conductivity type of 5 x 10^{18} cm^{-3} or less.

7. The semiconductor device according to claim 1, wherein

said body region potential setting portion includes a semiconductor region for body fixation of the second conductivity type formed together with said source region.

8. The semiconductor device according to claim 1, wherein

said partial isolation film lower semiconductor region has the second conductivity type and is formed in contact with said body region,

said semiconductor device further comprising:

an element formation region outside body region of a first conductivity type provided outside said element formation region of said SOI layer and being capable of externally fixing an electric potential, said element formation region outside body region being formed in contact with said partial insulating film lower semiconductor region.

9. The semiconductor device according to claim 1, wherein

said source and drain regions have such depths as to reach said buried insulating layer.

10. The semiconductor device according to claim 1, wherein

said source and drain regions have such depths that a depletion layer extended from said source and drain regions does not reach said buried insulating layer during a normal operation.

11. The semiconductor device according to claim 1, wherein

said source and drain regions have such depths that said buried insulating layer is not reached and a depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

12. The semiconductor device according to claim 1, wherein

said drain region has a greater depth than that of said source region and has such a depth that a depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

13. A semiconductor device having an SOI structure including a semiconductor substrate , a buried insulating layer and an SOI layer , comprising:

first and second semiconductor regions of a predetermined conductivity type provided in an element formation region of said SOI layer; and

a partial insulating film provided in an upper layer portion of said element formation region and a partial insulating film lower semiconductor region of a predetermined conductivity type to be a part of said element formation region in a lower layer portion of said element formation region,

wherein said partial insulating film lower semiconductor region is electrically connected to said first and second semiconductor regions to constitute a resistive element.

14. The semiconductor device according to claim 13, further comprising:

a complete insulating film provided through said SOI layer for isolating said element formation region.

15. The semiconductor device according to claim 13, wherein

said element formation region other than said partial insulating film and said first and second semiconductor regions is a part of a region where said resistive element is to be formed.

16. The semiconductor device according to claim 13, wherein

said resistive element includes a load resistor of an SRAM memory cell.

17. A semiconductor device having an SOI structure including a semiconductor substrate , a buried insulating layer and an SOI layer , comprising:

first and second element formation regions provided in said SOI layer;

a partial isolation region including a partial insulating film provided in an upper layer portion of said SOI layer and a semiconductor region to be a part of said SOI layer which is provided under said partial insulating film and serving to isolate said first and second element formation regions from each other; and

first and second MOS transistors formed in said first and second element formation regions, respectively,

wherein at least one of a structure of a body region, a structure of a gate electrode and presence/absence of body potential fixation in said first and second MOS transistors is varied to make transistor characteristics of said first and second MOS

transistors different from each other.

18. A semiconductor device having an SOI structure including a semiconductor substrate , a buried insulating layer and an SOI layer , comprising:

first and second element formation regions provided in said SOI layer;

a partial isolation region including a partial insulating film provided in an upper layer portion of said SOI layer and a semiconductor region to be a part of said SOI layer which is provided under said partial insulating film and serving to isolate said first element formation region from other regions;

a complete isolation region including a complete insulating film provided through said SOI layer and serving to isolate said second element formation region from other regions;

a first MOS transistor formed in said first element formation region; and

a second MOS transistor formed in said second element formation region,

wherein said first and second MOS transistors have different transistor characteristics.

19. A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing an SOI substrate having an SOI structure including a semiconductor substrate , a buried insulating layer and an SOI layer ;

(b) selectively forming a partial insulating film in an upper layer portion of said SOI layer, said partial insulating film constituting a partial isolation region for isolating first and second element isolation regions in said SOI layer together with a semiconductor region to be a part of said SOI layer which is provided under said partial insulating film;

and

(c) forming first and second MOS transistors in said first and second element formation regions,

wherein at said step (c), at least one of a structure of a body region, a structure of a gate electrode and presence/absence of body potential fixation in said first and second MOS transistors is varied to make transistor characteristics of said first and second MOS transistors different from each other.

20. A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing an SOI substrate having an SOI structure including a semiconductor substrate , a buried insulating layer and an SOI layer ;

(b) selectively forming a partial insulating film in an upper layer portion of said SOI layer, said partial insulating film constituting a partial isolation region for isolating said first element isolation region from other regions together with a semiconductor region to be a part of said SOI layer which is provided under said partial insulating film;

(c) selectively forming a complete insulating film through said SOI layer, said complete isolating film constituting a complete isolation region for isolating said second element formation region from other regions,

(d) forming a first MOS transistor in said first element formation region; and

(e) forming a second MOS transistor in said second element formation region,

wherein said steps (d) and (e) are performed such that said first and second MOS transistors have different transistor characteristics.